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Amendments to the Claims

Please cancel Claims 10 and 17, please amend Claims 1, 2, 4-6, 12, 13, 18 and 19, and please add new Claims 21 and 22 as follows:

1. (Currently amended) A method for fabricating one or more MOS transistors, the method comprising the steps of:

forming a buffer oxide layer on a semiconductor substrate having an isolation layer;

conducting ion implantations for well formation and field stop formation in an active region of the substrate through the buffer oxide layer;

removing the buffer oxide layer;

forming a sacrificial oxide layer on the semiconductor substrate;

patterning the sacrificial oxide layer to form a trench defining a gate electrode forming region; and

conducting ion implantations for threshold voltage adjustment and punch stop formation in the semiconductor substrate area under the trench.

2. (Currently amended) A method for fabricating one or more MOS transistors, the method comprising the steps of:

forming a buffer oxide layer on a semiconductor substrate having an isolation layer;

conducting ion implantations for well formation and field stop formation in an active region of the substrate through the buffer oxide layer;

removing the buffer oxide layer;

forming a sacrificial oxide layer on the semiconductor substrate;

patterning the sacrificial oxide layer to form a trench defining a gate electrode forming region;

conducting ion implantations for threshold voltage adjustment and punch stop formation in the semiconductor substrate area exposed by the trench;

forming a gate oxide layer on the exposed surface of the substrate;

forming a gate electrode layer on the sacrificial oxide layer so as to completely fill the trench;

polishing the gate electrode layer until the surface of the sacrificial oxide layer is exposed, so as to form a gate electrode;

removing the sacrificial oxide layer;

forming an LDD region in the surface of the substrate at both side portions of the gate electrode;

forming spacers on both side walls of the gate electrode; and

forming source/drain regions in the surface of the substrate at both side portions of the gate electrode including the spacers.

3. (Previously presented) The method for fabricating MOS transistors as claimed in claim 1, wherein ion implantation for punch stop formation is conducted only in the semiconductor substrate area under the trench.

4. (Currently Amended) The method for fabricating MOS transistors as claimed in claim 1, wherein the sacrificial oxide layer comprises a chemical vapor deposition (CVD) oxide layer.

5. (Currently Amended) The method for fabricating MOS transistors as claimed in claim 1, wherein the sacrificial oxide layer has a thickness ranging between 500Å and 1000Å.

6. (Currently Amended) The method for fabricating MOS transistors as claimed in claim 1, wherein the patterning of the sacrificial oxide layer comprises wet-etching the sacrificial oxide layer.

7. (Previously presented) The method for fabricating MOS transistors as claimed in claim 1, wherein ions implanted for well formation and field stop formation comprise boron, phosphorous or Arsenic.

8. (Previously presented) The method for fabricating MOS transistors as claimed in claim 1, wherein ion implantation for field stop formation is conducted at a sufficient energy to form a barrier below a source /drain junction.

9. (Previously presented) The method as claimed in claim 2, wherein ion implantation for punch stop formation is conducted only in the semiconductor substrate area exposed by the trench.

10. (Canceled)

11. (Previously presented) The method as claimed in claim 2, wherein the sacrificial oxide layer comprises a chemical vapor deposition (CVD) oxide layer.

12. (Currently Amended) The method as claimed in claim 2, wherein the sacrificial oxide layer has a thickness ranging between 500Å and 1000Å.

13. (Currently Amended) The method as claimed in claim 2, wherein the patterning of the sacrificial oxide layer comprises wet-etching the sacrificial oxide layer.

14. (Previously presented) The method as claimed in claim 2, wherein ions implanted for well formation and field stop formation comprise boron, phosphorous or Arsenic.

15. (Previously presented) The method as claimed in claim 2, wherein ion implantation for field stop formation is conducted at a sufficient energy to form a barrier below a source/drain junction.

16. (Previously presented) The method as claimed in claim 2, wherein said gate electrode layer comprises polysilicon.

17. (Canceled)

18. (Currently Amended) The method as claimed in claim 1, wherein the sacrificial oxide layer consists essentially of an oxide layer.

19. (Currently Amended) The method as claimed in claim 18, wherein the sacrificial oxide layer has a thickness ranging between 500Å and 1000Å.

20. (Previously presented) A method for fabricating a MOS transistor, comprising the steps of:

conducting ion implantations for threshold voltage adjustment and punch stop formation in an exposed semiconductor substrate area, said semiconductor substrate having an isolation layer therein and a patterned sacrificial oxide layer thereon, the patterned sacrificial oxide layer having a trench therein (i) defining a gate electrode forming region and (ii) exposing said exposed semiconductor substrate area;

forming a gate electrode in the trench;

removing the patterned sacrificial oxide layer;

forming an LDD region in the substrate at side portions of the gate electrode;

forming spacers on side walls of the gate electrode; and

forming source/drain regions in areas of the substrate not covered by the gate electrode and the spacers.

21. (New) The method as claimed in claim 20, wherein the sacrificial oxide layer consists essentially of an oxide layer.

22. (New) The method as claimed in claim 20, wherein the sacrificial layer comprises a chemical vapor deposition (CVD) oxide layer.